REMARKS

Claims 1-18 and 22-23 are pending in the present application. Claims 1, 8, 10, 18, 22, and 23 have been amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation, Claims 1, 2, and 4-9

The examiner has rejected claims 1, 2, and 4-9 under 35 U.S.C. § 102(e) as being anticipated by *Gholizadeh et al.*, (U.S. Patent No. 5,369,737). This rejection is respectfully traversed.

With regard to claim 1, the examiner states:

> As per claim 1, Gholizadeh discloses an apparatus for optimizing processing of graphics data (column 6 lines 40-65), the apparatus comprising: a plurality of logic units (fig 3, #'s 76, 72, 74), wherein the plurality of logic units are used to perform a graphics operation in which a set of constants is required for the graphics operation (column 6 lines 40-65); a first set of connections connecting the plurality of logic units to each other (fig 3), wherein the first set of connections are used to configure the plurality of logic units to determine the set of constants (column 6 lines 40-65); a second set of connections connecting the plurality of logic units (fig 3), wherein the second set of connections (to the lookup table) configure the plurality of logic units to perform the graphics operation in which the graphics operation using the constants is determined through the first set of connections (column 6 lines 40-65).

(*Office Action*, dated January 30, 2004, page 2).

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Amended independent claim 1, which is representative of independent claim 22, reads as follows:

> 1. An apparatus for optimizing processing of graphics data, the apparatus comprising:
>
> a plurality of logic units, wherein the plurality of logic units are used to perform a graphics operation in which a set of constants is required for the graphics operation;
>
> a first set of connections connecting the plurality of logic units to each other, wherein the first set of connections are used to configure the plurality of logic units to calculate the set of constants; and

> a second set of connections connecting the plurality of logic units, wherein the second set of connections configure the plurality of logic units to perform the graphics operation in which the graphics operation using the constants is calculated through the first set of connections.

Gholizadeh does not teach each and every feature of the presently claimed invention as recited in amended claim 1. Claim 1 recites having a first set of connections connecting the plurality of logic units to each other, wherein the first set of connections are used to configure the plurality of logic units to calculate the set of constants. Claim 1 also recites having a second set of connections connecting the plurality of logic units, wherein the second set of connections configure the plurality of logic units to perform the graphics operation in which the graphics operation using the constants is calculated through the first set of connections. Thus, claim 1 recites using connected logic units to calculate constants and then perform a graphics operation using the calculated constants.

The examiner points to the following section of *Gholizadeh* as teaching having a set of connections for configuring the logic units to determine the constants:

> Referring to FIG. 3, each pixel processor channel 40, 42, 44 (for example, red channel 42) comprises a 24 bit by 32 line register file 70, a fixed-point multiplier (MUL) 72 and a fixed point, 24 bit arithmetic logic unit (ALU) 74 for calculating and normalizing each pixel normal and evaluating illumination equation (1) for each pixel 66 using its normalized normal vector N. Specifically, register file 70 receives the constants of equation (1) (i.e., I.sub.a, K.sub.d, L, H, K.sub.s), pixel data (such as vertex normals N), the series expansion coefficients and triangle interpolation constants (i.e., A, B, C from equation (3)) computed as preprocessing steps by graphics processor 34. These quantities and their calculation are discussed in detail below. One output 71 of register file 70 is connected to the "B" inputs of multiplexers (MUXes) 76, 77. The output of MUX 76 is applied as the "A" operand to MUL 72. The "M" operand of MUL 72 is provided by register file output 73. The (product of operands A and M produced by MUL 72 is applied to the "A" input of MUX 77. The output of MUX 77 is connected to the "A" input of ALU 74, the input of which is supplied by output 75 of register file 70. MUXes 76, 77, MUL 72, and ALU 74 are controlled by controller 46 in response to commands from graphics processor 34, either via input interface 38 or directly on bus 35.

Gholizadeh, column 6, lines 40-65. In this portion of *Gholizadeh*, the cited reference describes one channel of a plurality of channels in the pixel processor system. The

components of each channel, which include a multiplier (MUL) and an arithmetic logic unit (ALU), are used to perform the graphics operation (normalization) for each pixel. Thus, the graphics operation (pixel normalization calculation) is performed by the components (MUL and ALU) in each channel.

However, the passage also teaches that the components (MUL and ALU) of the channel use constants in the equations for the normalization operation. The passage teaches that the constants to be used in the equation are received by the register unit **70** from graphics processor **34**. These constants are "computed as preprocessing steps by graphics processor **34**" (*Gholizadeh*, column 6, lines 51-52). Thus, the graphics processor **34** is used to calculate the constants used in the graphics operation, rather than the logic units in the pixel processor channel.

For example, Figure 1 of *Gholizadeh* illustrates the pixel processor system:

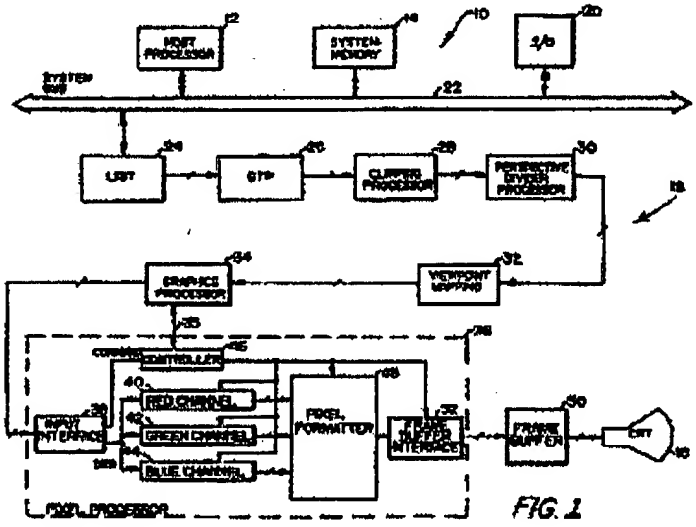

FIG. 1

As can been seen from Figure 1, the graphics processor **34** is not a logic unit within the pixel processor channels **40**, **42**, or **44**. The graphics processor itself calculates the constants to be used in the graphics operation and provides these constants as inputs to the logic units within the pixel processor channel. As such, there is no teaching in *Gholizadeh* of a configuration of connections between the logic units for calculating the constants. Thus, *Gholizadeh* fails to teach using a first set of connections to configure the plurality

of logic units to calculate the set of constants as recited in claim 1 of the present invention.

Furthermore, *Gholizadeh* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Gholizadeh* actually teaches away from the presently claimed invention because it teaches having graphics processor **34** calculate the set of constants as opposed to using a first set of connections to configure the plurality of logic units to calculate the set of constants as in the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement *Gholizadeh* and using a first set of connections to configure the plurality of logic units to calculate the set of constants, one of ordinary skill in the art would not be led to modify *Gholizadeh* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Gholizadeh* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

Therefore, applicants submit that *Gholizadeh* does not teach all elements of rejected independent claim 1. Claims 2 and 4-9 are dependent claims depending from independent claim 1. Applicants have already demonstrated claim 1 to be in condition for allowance. Applicants respectfully submit that claims 2 and 4-9 are also allowable, at least by virtue of their dependency on allowable claims.

Therefore, the rejection of claims 1, 2, and 4-9 under 35 U.S.C. § 102 has been overcome.

II. 35 U.S.C. § 103, Obviousness, Claim 3

The examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over *Gholizadeh* in view of *Rohner* (U.S. Patent No. 6,064,392). This rejection is respectfully traversed.

Claim 3 is a dependent claim depending from claim 1. Claim 3 is patentable over the cited references because the combination of *Gholizadeh* with *Rohner* would not reach the presently claimed invention. The features relied upon as being taught in *Gholizadeh* are not taught or suggested by that reference, as explained above in the response to the

rejection of claim 1. As a result, a combination of these references would not reach the claimed invention in claim 3.

Therefore, the rejection of claim 3 under 35 U.S.C. § 103 has been overcome.

III. 35 U.S.C. § 103, Obviousness, Claims 10-12 and 14-18

The examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over *Lindholm et al.*, (U.S. Patent No. 6,198,488) in view of *Gholizadeh*. This rejection is respectfully traversed.

With regard to claim 10, the examiner states:

> As per claim 10, Lindholm et al discloses a graphics pipcline (fig 1A) comprising: an input (fig 1A), wherein the input receives graphics data (fig 1A); an output (fig 1A), wherein the output transmits processed graphics data (fig 1A); and a plurality of stages (visibility logic, fog, etc.), wherein s first stage within the plurality of stages is connected to the input and a last stage within the plurality of stages is connected to the output, wherein s selected stage within the plurality of stages includes a plurality of modes of operation (fig 1A). However, Lindholm et al does not disclose modes of operation in which the selected stage is configured to determine constants for use in performing a graphics operation and in which the selected stage is configured to perform the graphics operation using the constants. This disclosed in Gholizadeh et al in column 6 lines 40-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate constants because this would increase processing speed by not having to regenerate them every time they are needed.

(*Office Action*, page 4).

For an invention to be prima facie obvious, the prior art must teach or suggest all claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Amended independent claim 10 reads as follows:

> 10. A graphics pipeline comprising:
> an input, wherein the input receives graphics data;
> an output, wherein the output transmits processed graphics data; and
> a plurality of stages, wherein a first stage within the plurality of stages is connected to the input and a last stage within the plurality of stages is connected to the output, wherein a selected stage within the plurality of stages includes a plurality of modes of operation including:
> a first mode of operation in which the selected stage is configured to calculate constants for use in performing a graphics operation; and

a second mode of operation in which the selected stage is configured to perform the graphics operation using the constants calculated through the first mode of operation.

Claim 10 is patentable over the cited references because neither *Lindholm* nor *Gholizadeh*, either alone or in combination, teaches or suggests the features of claim 10. Claim 10 recites a plurality of modes of operation including a first mode of operation in which a selected stage is configured to calculate constants for use in performing a graphics operation and a second mode of operation in which the selected stage is configured to perform the graphics operation using the constants calculated through the first mode of operation.

Lindholm teaches a graphics pipeline system for graphics processing, which includes a transform module adapted for being coupled to a vertex attribute buffer (VAB) for receiving attribute data. The transform module transforms the vertex data from object space to screen space. A lighting module is coupled to the transform module for performing lighting operations on the vertex data received from the transform module. A rasterizer is also coupled to the lighting module for rendering vertex data received from the lighting module (*Lindholm*, Abstract).

Applicants agree with the examiner that *Lindholm* does not teach modes of operation in which the selected stage is configured to determine constants for use in performing a graphics operation and in which the selected stage is configured to perform the graphics operation using the constants.

Gholizadeh does not cure the deficiencies of *Lindholm*. The examiner asserts that column 6, lines 40-65 of *Gholizadeh* teaches "modes of operation in which the selected stage in configured to determine constants for use in performing a graphics operation and in which the selected stage is configured to perform the graphics operation using the constants" (*Office Action*, page 4). However, all of the features relied upon as being taught in *Gholizadeh*, such as having a first mode of operation in which the selected stage is configured to calculate constants for use in performing a graphics operation, are not taught or suggested by that reference, as explained above in the response to the rejection of claim 1.

For example, claim 10 recites a selected stage having two modes of operation: one configured to calculate constants for use in performing a graphics operation, and another configured to perform the graphics operation using the constants. Thus, the selected stage both calculates constants and performs the graphics operation. Consequently, the logic units in *Gholizadeh*, which receive inputs from the input interface, cannot be a selected stage in terms of claim 10. Although the logic units within a pixel processor channel may perform the graphics operation in one mode of operation, the logic units do not have another mode of operation in which they calculate constants to be used in the graphics operation, as explained above in the response to the rejection of claim 1. Thus, the logic units within the pixel processor channel in *Gholizadeh* are not the selected stage having two modes of operation as recited in claim 10. Consequently, *Gholizadeh* fails to teach having a selected stage configured to calculate constants for use in performing graphics operation and to perform the graphics operation using the constants.

Thus, in view of the above, neither *Lindholm* and *Gholizadeh*, either alone or in combination, teaches or suggests the features of independent claims 1 and 10. Claims 11, 12, and 14-18 are dependent claims depending on independent claim 10. Applicants have already demonstrated claim 10 to be in condition for allowance. Applicants respectfully submit that claims 11, 12, and 14-18 are also allowable, at least by virtue of their dependency on an allowable claim.

Thus, the rejection of claims 10-12 and 14-18 under 35 U.S.C. § 102(e) has been overcome.

IV. 35 U.S.C. § 103, Obviousness, Claim 13

The examiner has rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over *Lindholm et al.*, (U.S. Patent No. 6,198,488) in view of *Gholizadeh* and further in view of *Rohner*. This rejection is respectfully traversed.

Claim 13 is a dependent claim depending from claim 10. Claim 13 is patentable over the cited references because the combination of *Lindholm* and *Gholizadeh* with *Rohner* would not reach the presently claimed invention. The features relied upon as being taught in *Gholizadeh* are not taught or suggested by that reference, as explained

above in the response to the rejection of claim 10. As a result, a combination of these references would not reach the claimed invention in claim 13.

Therefore, the rejection of claim 13 under 35 U.S.C. § 103 has been overcome.

V. 35 U.S.C. § 103, Obviousness, Claims 22-23

The examiner has rejected claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over *Cobb et al.*, (U.S. Patent No. 6,603,474) in view of *Gholizadeh*. This rejection is respectfully traversed.

As per claims 22 and 23, the examiner states:

> As per claim 22, Cobb et al discloses an input configured to receive graphics data (column 1 lines 30-34); a raster engine connected to the input and to the frame buffer, wherein the raster engine rasterizes the processed graphics data for display (column 4 lines 32-38); a geometry engine connected to the raster engine (column 4 lines 32-38), processes the graphics data to the raster engine to form the processed graphics data (column 4 lines 32-38), and returns the processed graphics data to the raster engine and wherein the geometry engine includes a set of processing elements in which at least one processing element within the set of logic units (it is well known for geometry engines to include processing elements because you are processing geometry data). However, Cobb et al does not disclose in which the set of logic units is used to determine at least one constant for the equation used in the operation. This disclosed in Gholizadeh et al in column 6 lines 40-65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate constants because this would increase processing speed by not having to regenerate them every time they are needed.

(*Office Action*, page 5-6). Amended independent claim 22 reads as follows:

> 22. A graphics adapter comprising:
> an input configured to receive graphics data;
> a frame buffer, wherein processed graphics data is stored for display;
> a raster engine connected to the input and to the frame buffer, wherein the raster engine rasterizes the processed graphics data for display,
> a geometry engine connected to the raster engine, wherein the geometry engine receives graphics data from the raster engine, processes the graphics data to form the processed graphics data, and returns the processed graphics data to the raster engine and wherein the geometry engine includes a set of processing elements in which at least one processing element within the set of processing elements includes a set of

> logic units, in which the set of logic units is used to perform an operation on the graphics data using an equation and wherein a portion of the set of logic units is used to calculate at least one constant for the equation used in the operation.

Claim 22 is patentable over the cited references because the combination of *Cobb* with *Gholizadeh* would not reach the presently claimed invention. All of the features relied upon as being taught in *Gholizadeh*, such as using a portion of the set of logic units to determine at least one constant for the equation used in the operation, are not taught or suggested by that reference, as explained above in the response to the rejection of claim 1. As a result, a combination of these references would not reach the claimed invention in claim 22.

Furthermore, no teaching, suggestion, or incentive is present for combining *Cobb* and *Gholizadeh* as suggested by the examiner when the references are considered as a whole by one of ordinary skill in the art. *Cobb* recognizes the following:

> In general, a goal of 3D computer graphics is to create a 2D projection on a display screen of a three-dimensional model as viewed from a predetermined viewpoint in three-dimensional model space. One aspect of such a projection is the need to keep track of which objects are in front of other objects, and which are behind, when viewed from the viewpoint. This knowledge is necessary to ensure that, for example, a building in the foreground will properly occlude a building in the distance. This aspect of the rendering process is known as "occlusion culling".

Cobb, column 1, lines 15-24. *Cobb* is concerned with identifying visible and occluded objects in a data processing system.

The solution provided by *Cobb* is taught as follows:

> The present invention provides a method for displaying a drawing for a viewpoint in a data processing system wherein the drawing includes a set of objects. A plurality of bounding boxes and complexity data for the set of objects is received, wherein a bounding box and complexity data are associated with each object within the set of objects. Occluders within the set of objects are selected using the plurality of bounding boxes and complexity data. These occluders are used to identify visible objects from the set of objects for the viewpoint.

Cobb, column 1, line 66 to column 2, line 8. As can be seen, the solution provided by *Cobb* involves determining whether objects are visible in a scene from a given view.

In contrast, *Gholizadeh* is concerned with the normalization of vectors (e.g., those used to implement shading) associated with display pixels of computer-generated images. *Gholizadeh* recognizes the problem of performing one shading algorithm, the Phong algorithm, in real-time. The solution provided by *Gholizadeh* is taught as follows:

> Thus, in the invention, the calculation of the normalized normal vector and/or light vector (or vectors) at each pixel requires only a few simple operations, which may be rapidly performed (e.g. in a few machine cycles) with fixed point hardware or in software, thereby enabling Phong shading to be performed in real time. Further, the series expansion coefficients are generic-once initially determined, the coefficients apply to produce shading for all of the pixels within all of the polygons (i.e., triangles) used to represent the surfaces of a displayed image. This reduces the amount of preprocessing necessary to support Phong shading.

Gholizadeh, column 2, lines 3-25. As can be seen, the solution provided by *Gholizadeh* involves simplifying the operations needed to calculate the normalized vector at each pixel such that the calculation may be rapidly performed with fixed point hardware or in software, thereby enabling Phong shading to be performed in real time.

Thus, these two references are directed towards different problems and solutions when they are considered as a whole by one of ordinary skill in the art. As a result, no teaching, suggestion, or incentive is present for combining these references in the manner recited by the examiner. The combination of modifications can only be made through an improper use of hindsight with the benefit of applicant's disclosure as a template to piece together the teachings needed to reach the presently claimed invention in amended claim 22.

Since claim 23 depends from claim 22, the same distinctions between *Cobb* and *Gholizadeh* and the claimed invention in claim 22 apply for this claim. Applicants have already demonstrated claim 22 to be in condition for allowance. Applicants respectfully submit that claim 23 is also allowable, at least by virtue of its dependency on an allowable claim.

Therefore, the rejection of claims 22 and 23 under 35 U.S.C. §103 has been overcome.

VI. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 4/13/04

Respectfully submitted,

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